[0025] FIG. **13** is a plan view showing a variation on the device shown in FIG. **6**.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0026] Terms such as above, below, over, and so on as used herein refer to a semiconductor device orientated as shown in the figures and should be construed accordingly. It should also be appreciated that, because regions within a semiconductor device are defined by doping different parts of a semiconductor with differing impurities or differing concentrations of impurities, discrete physical boundaries between different regions may not actually exist in the completed device but instead regions may transition form one to another. Some boundaries as shown in the accompanying figures are of this type and are illustrated as abrupt structures merely for the assistance of the reader. The skilled artisan can readily determine with such gradients where to set boundaries for discrete functional diffusion regions in a semiconductor device.

[0027] As noted before, transistors have sometimes been used to provide electrostatic protection devices. However an integrated circuit may contain millions of transistors. The circuit designer wants to use as few process steps as possible in the fabrication of the integrated circuit since each additional masking and implanting step adds further cost. Also each step brings an increased error rate which reduces the yield of working devices formed on a wafer. Thus additional steps are preferably avoided. Given that the majority of transistors on a device will have a specific task, such as forming logic elements, then the transistor parameters are chosen so as to be appropriate for the majority task. Consequently the transistors that are formed are generally not suited for use in electrostatic discharge protection circuits, or give severely compromised performance.

[0028] FIG. **1** shows part of an integrated circuit **5**, according to one embodiment. The integrated circuit has a device, in this instance an input transistor **10** whose drain and source are connected to circuit components **12** and **14**, which may be any type of circuits with any function for the purpose of the present disclosure. A gate **16** of the transistor is connected to an input terminal **18** of the integrated circuit. The transistor **10** is susceptible to permanent damage due to high voltages of the input terminal **18**, for example electrostatic discharge if someone handling the integrated circuit **5** had become charged by walking over a nylon carpet.

[0029] In order to protect the transistor **10** from damage, an electrostatic protection device (or circuit) **20** is provided so as to limit the voltage excursions at the gate **16** of the transistor.

[0030] It is useful to consider the operation of an electrostatic discharge, ESD, protection device. Ideally, an electrostatic protection device should exhibit a controllable and selectable trigger voltage T. For input voltages having a magnitude less than the trigger voltage T, the device should be in a high-impedance (non-conducting) state. Once the trigger voltage magnitude has been exceeded the device should enter a low impedance state and start conducting.

[0031] The protection device may also offer "fold back" or "snap back" such that once it starts conducting, the voltage across the device reduces to a lower value. In this case, the device remains conducting, provided that the input voltage remains above a threshold magnitude, which may be called a "holding voltage".

[0032] FIG. **2** illustrates an operating characteristic of an electrostatic protection device. It can be seen that the ESD protection device does not pass any current until a trigger voltage T has been reached. The trigger voltage is less than a breakdown voltage B for the device being protected. Once the trigger voltage has been reached the ESD protection device starts conducting, and the voltage across the device falls back to a holding voltage H. Although in an ideal device current flow could then increase without the voltage across the device increasing, due to resistance within the device, the voltage increases slightly with increasing current in the region **30**. If the holding voltage is not outside the supply rail voltage range, then once the ESD protection device has switched on, it will not switch off. Once the voltage across the device has decreased below a holding voltage, H, the ESD protection device can return to a high impedance state, effectively switching off.

[0033] The inventors realized that for a given transistor fabrication process, it would be desirable for the trigger voltage and the holding voltage to be well controlled, and better still, adjustable. Doping concentrations and thermal budgets are already constrained by the function of the majority devices when those devices are simultaneously fabricated with ESD protection device(s). Therefore, those control parameters are not accessible to independently tailor ESD protection device performance. Fabrication steps to tailor doping just for ESD protection devices are costly, and it is not feasible to separate thermal budgets for different devices on the same substrate. Thus, it may be useful to control other device parameters and internal transistor processes.

[0034] Consider, for example, the structure of a vertically formed NPN bipolar transistor. During device fabrication the semiconductor wafer exists as a slab whose width and length is much greater than its depth. A surface of the wafer is exposed to impurities for doping. The surface is regarded as an upper horizontal surface in a frame of reference that is adopted for the purposes of description. An exemplary prior-art transistor **60** is illustrated in FIG. **3**. The device shown in FIG. **3** represents a single transistor within an integrated circuit, which may have millions of transistors formed thereon. The active part of the transistor comprises an N^+ region **100** which acts as the collector of the transistor. The N type region is formed by doping the semiconductor with a donor impurity, as is well known to the person skilled in the art. The "+" symbol represents a region of relatively heavy doping. This, again, is a convention well known to and understood by the person skilled in the art. The N type region can be formed as a well within a P type substrate **80**. This gives rise to the formation of a PN junction well, which can be reverse biased so as to isolate the bulk of the transistor from other transistors within the integrated circuit. Alternatively, the transistor can be formed within a semiconductor well that is defined along its sides and bottom by a layer of silicon dioxide, as is known for silicon on insulator (SOI) fabrication. Connections are made to the collector region **100**. This is achieved by providing vertical N type regions **102** extending between the collector region **100** and the surface of the semiconductor. Metallic collector contacts **104** make galvanic contact with the N type semiconductor.

[0035] A further region of less heavily doped N type semiconductor **110** is provided above the collector **100**, and bounded by the vertical regions **102**. It contains a well of P^+ doped semiconductor which forms the base region **120** of the transistor. Finally, an emitter region **130** of N^+ doped semi-